**PRELIMINARY DESIGN REVIEW**

**Lafayette College**

**Department of Electrical and Computer Engineering**

Title: Wireless Network-WimpFi

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1. **Requirement checklist**

|  |  |  |
| --- | --- | --- |
| **Description** | **Test Method** | **Detailed Results** |
| 1. Module Interface | Code Inspection | |  | | --- | | We added few extra inputs and outputs compared to the Lab design, i.e.  1. Check for error in PREAMBLE-SFD, bit and EOF via correlator use  2. Added Transmitter from Lab3 for switching in between RealTerm data input and user given switches data input  3. Added a synching counter between the mx\_test and Manchester transmitter to know when mx\_test finished sending data to BRAM  4. Choose destination address in mx\_test based on user input from switches on Nexys board  5. Use single pulser module for ready input in the transmitter adapter  6. Added a time counter for use with transmitter adapter to count no. of bytes transmitted | |
| 2 . Module function: integrates the complete Manchester transmitter, receiver, asynchronous transmitter and receiver, receiver and transmitter adapters, fifo and transceiver interface developed in previous labs, and an additional BRAM and CRC module | Demonstration in oscilloscope and test bench simulation and Nexys4DDR board:  **TEST BENCH**  1. Display of data received  2. Display of PREAMBLE-SFD transition  3. Display of EOF transition  4. Proper display of system reset  5. Proper display of destination address  6. proper display of source address  7. Proper display of type  8. Proper display of FCS  9. Proper display of ACK frame  10. Proper display of 252 bytes of data when BRAM full  11. Proper display of read pointer to destination address at beginning of loading BRAM  12. Proper display of write pointer to the type address at beginning of loading BRAM  13. Proper assertion of full when BRAM write pointer is at address 255  14. Proper de-assertion of cardet when BRAM write pointer is at address 255  15. Display of PREAMBLE-SFD-DESTINATION ADDR-SOURCE ADDR-TYPE ADDR-DATA-EOF for type 0 frame  16. Display of PREAMBLE-SFD-DESTINATION ADDR-SOURCE ADDR-TYPE ADDR-DATA-FCS-EOF for type 1 frame  17. Display of PREAMBLE-SFD-DESTINATION ADDR-SOURCE ADDR-TYPE ADDR-FCS\_EOF for type 3 frame  18. Display of type 1 and type 3 for type 3 frame  19. Proper display of rdy when BRAM not empty  20. Proper display of rerrcnt when receival error occurs  21. Proper display of xerrcnt when transmission error occurs  22. Proper detection of frame types from data BRAM stored in BRAM  23. Proper ignore of frame in the case of erroneous mac address for destination  24. proper display of frame checking sequence upon zero crc  25. Proper display of frame checking sequence when crc is non-zero  26. proper increment of rerrcnt counter in case of non-zero crc  27. Proper display of ACK in case of broadcast address  28. Proper display of baudrate from given bit rate  29. Proper display of random backoff for type 0 through time counter | **OSCILLOSCOPE & FPGA HARDWARE**  1. Proper display of cardet output on oscilloscope at EOF  2. Proper display of system reset on seven segment display on Nexys board  3. Proper display of manchester receiver data on seven segment display  4. Proper display of full, empty and ready on LEDs on Nexys board  5. Proper display of received data on the oscilloscope  6. Proper receival of other station transmission on realterm  7. Proper receival of other station transmission on Nexys board  8. Display of PREAMBLE-SFD transition on oscilloscope  9. Display of EOF transition on oscilloscope  10. Proper display of destination address on oscilloscope  11. proper display of source address on oscilloscope  12. Proper display of type on oscilloscope  13. Proper display of FCS on oscilloscope  14. Proper display of ACK frame on oscilloscope  15. Proper display of 252 bytes of data when BRAM full on Realterm  16. Proper display of destination address on Realterm  17. proper display of source address on oscilloscope  18. Proper display of type on Realterm  19. Proper display of FCS on Realterm  20. Proper display of ACK frame on Realterm  21. Proper display of PREAMBLE-SFD-DESTINATION ADDR-SOURCE ADDR-TYPE ADDR-DATA-EOF for type 0 frame on oscilloscope  22. Proper display of PREAMBLE-SFD-DESTINATION ADDR-SOURCE ADDR-TYPE ADDR-DATA-FCS-EOF for type 1 frame frame on oscilloscope  23. Proper display of PREAMBLE-SFD-DESTINATION ADDR-SOURCE ADDR-TYPE ADDR-FCS\_EOF for type 3 frame frame on oscilloscope  24. Proper display of type 1 and type 3 for type 3 frame frame on oscilloscope  24. Proper detection of frame types from data BRAM stored in BRAM on oscilloscope  25. Proper display of baudrate from given bit rate on oscilloscope |
| 3. Uses Nexys4 board 100Mhz clock; all flip-flop clock inputs tied directly to this signal | Code inspection  *(all the instances of the clk use in the modules are provided)* | Provide the section in vivado synthesis report |
| 4. Contains no latches | Inspection of Synthesis Report | Provide the section in vivado synthesis report |
| 5. Test circuit – show test that test circuit functions properly to exercises circuit. | Demonstration in hardware  1. Proper display of cardet output on oscilloscope  2. Proper display of reset on seven segment display on Nexys board  3. Proper display of manchester receiver data on seven segment display  4. Proper display of full, empty and ready on LEDs on Nexys board  5. Proper display of received data on the oscilloscope  6. Demonstrate the transition from asynchronous transmitter to RealTerm input  7. Proper display of transmission from Manchester transmitter to other stations  8. Display of PREAMBLE-SFD transition on oscilloscope  9. Display of EOF transition on oscilloscope  10. Proper display of destination address on oscilloscope  11. proper display of source address on oscilloscope  12. Proper display of type on oscilloscope  13. Proper display of FCS on oscilloscope  14. Proper display of ACK frame on oscilloscope  15. Proper display of 252 bytes of data when BRAM full on Realterm  16. Proper display of destination address on Realterm  17. proper display of source address on oscilloscope  18. Proper display of type on Realterm  19. Proper display of FCS on Realterm  20. Proper display of ACK frame on Realterm  21. Proper display of PREAMBLE-SFD-DESTINATION ADDR-SOURCE ADDR-TYPE ADDR-DATA-EOF for type 0 frame on oscilloscope  22. Proper display of PREAMBLE-SFD-DESTINATION ADDR-SOURCE ADDR-TYPE ADDR-DATA-FCS-EOF for type 1 frame frame on oscilloscope  23. Proper display of PREAMBLE-SFD-DESTINATION ADDR-SOURCE ADDR-TYPE ADDR-FCS\_EOF for type 3 frame frame on oscilloscope  24. Proper display of type 1 and type 3 for type 3 frame frame on oscilloscope  24. Proper detection of frame types from data BRAM stored in BRAM on oscilloscope  25. Proper display of baudrate from given bit rate on oscilloscope  26. Use smaller size BRAM to facilitate fitting design into smaller XC7S15 FPGA  27. Parametrize mac address to facilitate reconfiguration of mac address  28. Proper inspection of the design and copyrights of the Nortel Manchester Decoder patent relative to our own preliminary design  29. Proper display of fail-safe through the full variable added to the BRAM to stop further writing to the BRAM once required 255 bytes complete. 256th address will contain FCS, which shall be ignored  30. Detail check list of compliance with the EU RoHS directive for environmental sustainability, in choice of manufacturing material.  31. Given CRC and MEM modules shall be converted to system Verilog syntax. All previous modules are in system Verilog. | Demonstrate to Professor Nadovich |
| In submitting this checklist as part of our report, I/We certify that the tests described above were conducted and that the results of these tests are accurately described and represented. I/We understand that any misrepresentation of the tests or the results constitutes a violation of the College policy on academic dishonesty. | | |
| Name(s):Kemal Dilsiz & Zainab Hussein Date: 11/11/2016 | | |

1. **High-level Description**

Our design combines the manchester transmitter from Lab3 and manchester receiver implementation from this lab, asynchronous transmitter and receiver to form a complete network station. In addition, additional modules are included such as transmitter and receiver adapters, and storage modules such as BRAM.

Top level diagrams for the Manchester transmitter and receiver are shown in figure 1 and 2.

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Figure 1

Therefore, the data can be transmitted through the user input and also from the mx\_test module via changing the length. This would allow us to quickly change input and test it on the oscilloscope. The data received will be stored in FIFO for displaying in RealTerm via Async Serial Transmitter from lab2. This will make it so that we can check if our input is same as the output even when there is noise.

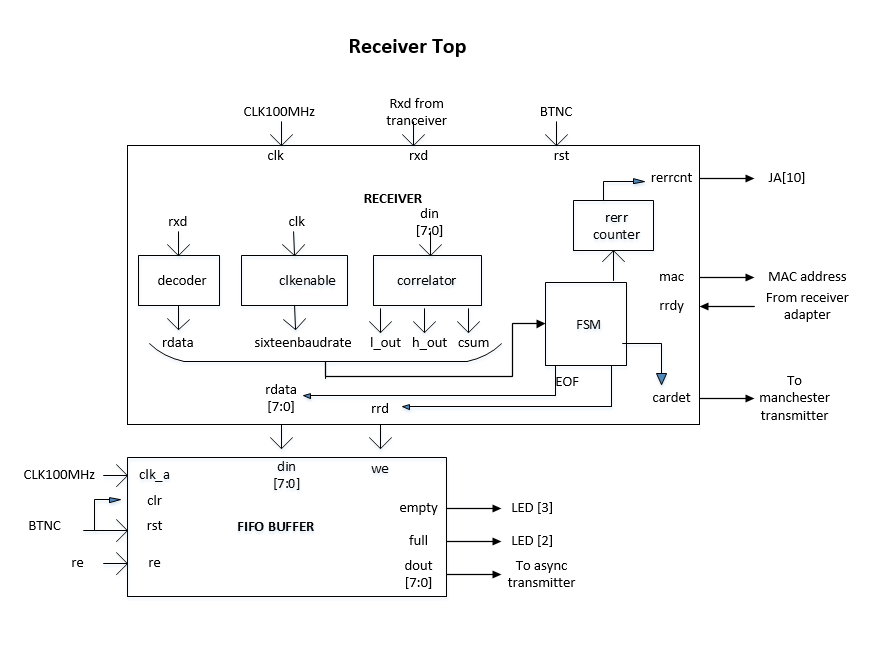


Figure 2

Design Alternatives:

1. In the transmitter module, have the BRAM come after the Fsm, this design would allow for the mx\_text to send data directly to the fsm before being stored in the BRAM. We decided against this approach because it is harder to know the amount of bytes sent to the BRAM, and would have to include the FCS in the BRAM, which is against design specification.
2. Have the BRAM as a separate module outside of the Manchester transmitter. We decided against this approach to better follow the interaction and dependencies of the variables with the controller state machine.
3. **Detailed Description**

Transmitter state machine is shown in figure 3, receiver state machine in figure 4, transmitter adapter in figure 5, receiver adapter in figure 6, BRAM logic in figure 7. The process of realizing the project can be summarized in the figures that follow.

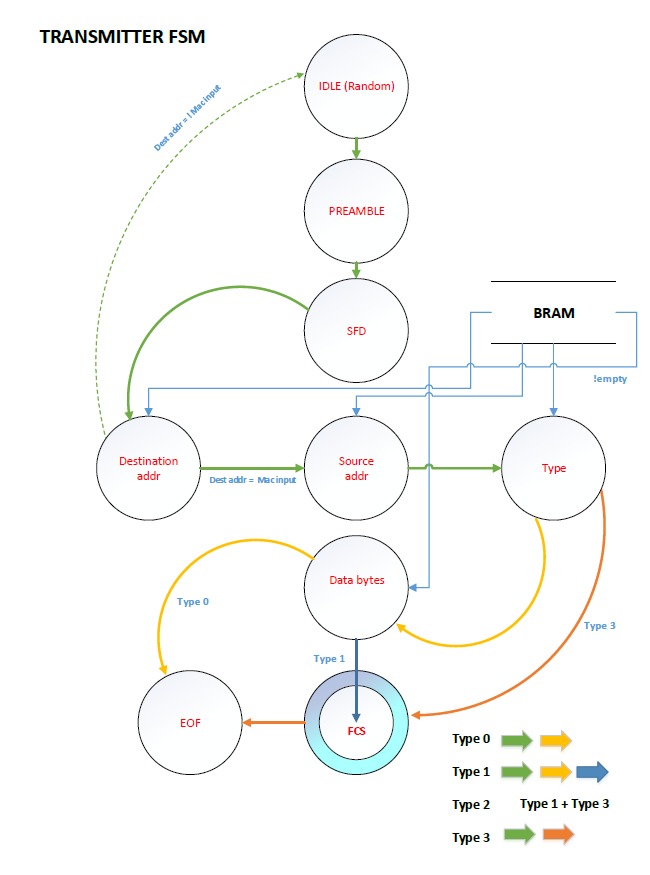


Figure 3

Receiver state machine

U:\Fall 2016\491\receiverfsm.png

Figure 4

U:\Fall 2016\491\TransmitterAdapter.png

Figure 5

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Figure 6

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Figure 7